Fujitsu 90nm Technology
Introduction

Fujitsu Limited.
2005.08
Fujitsu Advanced Technology
Fujitsu CMOS Technology Roadmap

CS100/CS100A (90nm)
- L actual=40-80nm
- SiOC(k:2.9) low-k
- Dual Damascene Cu

CS200/CS200A (65nm)
- L actual=30-50nm
- NCS (Nano-Clustering Silica)
90nm Technology Lineup

Operating Frequency vs. Power Consumption

CS100A_LL
Mobile
Consumer
Graphics
Network
FPGA

CS100A_G*
High-End MPU

*Supply only technology

Fujitsu Proprietary and Confidential
Proven track records of 90nm complex design and products (1)
- In House Application -

- Processors for PRIMEPOWER
  Achieves world-leading performance and reliability

- Chipset for PRIMEQUEST
  Achieves mainframe-class reliability and scalability
  Helped reduce development time

- Baseband chip for FOMA 3G mobile phones
  LSI power consumption reduced 50%
  (compared to existing tech)
High performance products

- 90nm complex design and products (2)

Low power products

- 90nm complex design and products (2)

30 Product Taped Out
200 prototype wafers delivered
Fujitsu 90nm - Key Features

- High Performance Transistors
  - Advanced Lithography and Etch technology to achieve 40nm Gate Length
  - Low Temperature Process for Shallow Junction
  - Process Optimization for High Carrier Mobility

- High density 6T SRAM
  - sub-1um² cell is available
  - *Dual Damascene Cu + Full Low-k
  - *Assy and packaging technology
    - Full Low-K + Pb free bump
      - Large pin count + Large die size**

- * High performance and high reliability.
- ** This combination can realize by only Fujitsu in the world.
1nm-thick Gate Oxide

Surface Cleaning

Normalized $g_m$ (mobility)

Electric Field [MV/cm]

Si substrate

Nitrided-SiO$_2$

Poly-Si

40% increase

After optimize

Before
Advantage of Fujitsu 90nm technology

Fujitsu is the World’s No.1 Leading Edge Process Technology Supplier

- One customer’s benchmark results show Fujitsu’s technology has higher performance and low power consumption compared with one of the standard foundry technologies.

<table>
<thead>
<tr>
<th>Speed and Power Comparison</th>
<th>Foundry A</th>
<th>Fujitsu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>100</td>
<td>125</td>
</tr>
<tr>
<td>Active Power</td>
<td>100</td>
<td>75</td>
</tr>
<tr>
<td>Stand-by Power</td>
<td>100</td>
<td>21</td>
</tr>
</tbody>
</table>
CS100A_LL process covers a *broad range* of requirement for both high performance and low leakage current.
Power/Delay estimation result
Assumption Logic : 1.7Mgate, SRAM : 8Mbit
Cu/Low-k Integration Technology

- Fourth-generation Cu wiring LSI
- Leading-edge Low-k technology

Wiring Pitch (µm)

0.18um  0.13um  90nm  65nm

Technology Node

CS80
*Cu-6 Layer
*FSG (k=3.6)

CS90A
*Cu-7 Layer
*Partial Low-k

CS100/100A
*Cu-10 Layer
*Full Low-k

CS200/201
*Cu-11 Layer
*Full Advanced Low-k
6T SRAM Cell

<CS80A / 180nm>
4.18um²
1.88
2.22

<CS90A/ 130nm>
1.98um²
1.20
1.65

<CS100A/ 90nm>
1.14um²
16 - 512Kbit

Conventional Type:
Symmetrical Type:
Verified
For Bigger size

0.917um²
32K - 8Mbit

Verifed
For Bigger size
Outlook of new fab.

World first semiconductor fab. with a micro vibration control & seismically isolated structure

Mie New Fab. Milestone

- Apr. 21, 2004
  Ceremony for sanctifying ground

- Nov. 20, 2004
  Completion of construction

- Apr. 1, 2005
  Formal operation starts

- Sept. 9, 2005
  Volume shipment
300mm foundry capacity for 90nm/65nm

Mie 300 mm Fab
Advanced technology production 2005/2H~

Akiruno TC 200mm
Advanced technology development and production

Leading-edge Technology
Fujitsu 90nm

Year

Capacity (200mm/month)

Capacity (300mm/month)

2004/2H 2005/1H 2005/2H 2006/1H 2006/2H 2007/1H 2007/2H

300mm Fab
Akiruno TC
Customers are satisfied with the Si verified IP.

Fujitsu provide extensive IP line up.

- High Speed I/O
- STD I/O
- SRAM
- I/F (USB 2.0 etc)
- AD/DA
- PLL

* Chip photo is not related on each IP.
Fujitsu Foundry Services
Fujitsu launched pure foundry business as primary to keep pace with market shift from ASIC to foundry.

This advertisement is published in “Nikkei electronics 2004 12-6, page 100-101”, which is one of the major magazine of electronics in Japan.

In 2005 April, Fujitsu has released the similar advertisement in U.S.A.

Fujitsu made foundry business division to focus the foundry business in 2004 June.
Customers’ needs are changing with evolution in LSI development. Customers require integrated design and engineering and flexible manufacturing capabilities.

Strong Appeal as New IDM Vendor

- System Design
- Logic Design
- Physical Design
- Foundry

New business opportunity (Technology & Engineering Service)

Fujitsu’s conventional LSI business
Customer can select service and biz model.
EDG in Japan

Iwate Plant
[Memory, Microcomputer, Logic]

FIM (Miyagi) Assembling

FIM (Aizu) Assembling & Test

Akiruno TC (Tokyo)
R&D (90nm

FIM (Gifu) Assembling & Test

FIM: Fujitsu
Integrated Microtechnology

All Rights Reserved, Copyright FUJITSU LIMITED 2005
SiExpress™ is a pre-production service where customers save cost by sharing mask sets and wafer, called multi-project-wafer. SiExpress™ service provides completely consistent samples which enable your real product’s performance evaluation.

Sample forms
• Bare Chips
• Package chips
Fab information system

~FF-eSERVE~

Secured accessibility
for world wide customers

Customers can access FJ foundry information through the Internet with high security
Fab information linked customer’s PO

Received PO

- Engineering docs
- Lot history
- Daily WIP
- Inprocess data
- WAT data
- SORT data
- Wafer Map
- Wafer Shipping info

- Assembly WIP
- LSI Shipping info

Customers can get FJ foundry information linked PO

FF-eSERVE

The fab information system of your own

Query Info

Customer
Why Fujitsu foundry?

- Fujitsu launched foundry biz.
- Provide 300mm capacity for “Foundry Customer”
- Customer can enjoy the Fujitsu’s high performance and low leakage 90nm technology.
- Matured 90nm device production
  - From high end to low power devices
  - Higher yield than other fab.
- Extensive IP line up
EDA tool vendor’s support

Cadence Foundry Program


Synopsys SPV Cafe

http://www.synopsys.com/cgi-bin/svp/lib/svp.cgi
## Standard Cell

### 1. Standard cell

#### 1-1. CS100A_LL

<table>
<thead>
<tr>
<th>Cell Height</th>
<th>Tr.</th>
<th>LL</th>
<th>STD</th>
<th>HS</th>
</tr>
</thead>
<tbody>
<tr>
<td>9grid</td>
<td>Now</td>
<td>Now</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td>12grid</td>
<td>Now</td>
<td>Now</td>
<td>Now</td>
<td></td>
</tr>
</tbody>
</table>

#### 1-2. CS100HP

<table>
<thead>
<tr>
<th>Cell Height</th>
<th>Tr.</th>
<th>HiVT</th>
<th>STD</th>
<th>HS</th>
</tr>
</thead>
<tbody>
<tr>
<td>9grid</td>
<td>3Q / 2005</td>
<td>3Q / 2005</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

LL : Low-Leak Tr. , STD : Standard Tr. , HS : High-Speed Tr. , HiVT : High-Vth Tr.
## I / O Cell

### 2. I/O cell

#### 2-1. CS100A_LL

<table>
<thead>
<tr>
<th>Interface</th>
<th>Status</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V LVCMOS</td>
<td>Now</td>
<td>(63cells) for 3.3V Process</td>
</tr>
<tr>
<td>3.3V PCI</td>
<td>Now</td>
<td>(5cells, 66/33MHz) for 3.3V Process</td>
</tr>
<tr>
<td>SSTL-2</td>
<td>Now</td>
<td>(5cells, 400Mbps) for 3.3V Process</td>
</tr>
<tr>
<td>LVDS</td>
<td>4Q / 2005</td>
<td>(5cells, 333MHz) for 3.3V Process</td>
</tr>
</tbody>
</table>

#### 2-2. CS100HP

<table>
<thead>
<tr>
<th>Interface</th>
<th>Status</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5V LVCMOS</td>
<td>3Q / 2005</td>
<td>(TBD) for 2.5V Process</td>
</tr>
</tbody>
</table>
# Memory

## 3. SRAM / ROM / Register File

<table>
<thead>
<tr>
<th>Type</th>
<th>CS100A_LL</th>
<th>CS100HP</th>
<th>Status</th>
<th>Tr. Type (Cell / Peripheral)</th>
<th>Status</th>
<th>Tr. Type (Cell / Peripheral)</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1RW SRAM</td>
<td>LL / LL</td>
<td>Now</td>
<td>HiVT / HiVT</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / STD</td>
<td>Now</td>
<td>HiVT / STD</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / HS</td>
<td>Now</td>
<td>HiVT / HS</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2RW SRAM</td>
<td>LL / LL</td>
<td>Now</td>
<td>HiVT / HiVT</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / STD</td>
<td>Now</td>
<td>HiVT / STD</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / HS</td>
<td>Now</td>
<td>HiVT / HS</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROM</td>
<td>LL / LL</td>
<td>Now</td>
<td>HiVT / HiVT</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / HS</td>
<td>Now</td>
<td>HiVT / STD</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1R1W Reg. File</td>
<td>LL / LL</td>
<td>Now</td>
<td>HiVT / HiVT</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / STD</td>
<td>Now</td>
<td>HiVT / STD</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / HS</td>
<td>Now</td>
<td>HiVT / HS</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2R2W Reg. File</td>
<td>LL / LL</td>
<td>Now</td>
<td>HiVT / HiVT</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / STD</td>
<td>Now</td>
<td>HiVT / STD</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LL / HS</td>
<td>Now</td>
<td>HiVT / HS</td>
<td>On demand</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*1 : Virage’s IP

LL : Low-Leak Tr. , STD : Standard Tr. , HS : High-Speed Tr. , HiVT : High-Vth Tr.
### I/F Macro, ARM

#### I/F Macro

<table>
<thead>
<tr>
<th>Macro</th>
<th>Functions</th>
<th>Specifications</th>
<th>Design completion</th>
<th>Evaluation completion (SiliconProven)</th>
<th>Note (Procurement or Development)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 USB2.0 Device</td>
<td>USB2.0(HS) Device PHY</td>
<td>Now</td>
<td>2005/5/E</td>
<td>2005/8/E</td>
<td>Development</td>
</tr>
<tr>
<td>2 USB2.0 Host</td>
<td>USB2.0(HS) Host PHY</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>Development</td>
</tr>
<tr>
<td>3 USB2.0 OTG</td>
<td>USB2.0(HS) OTG PHY</td>
<td>Now</td>
<td>2005/7/E</td>
<td>TBD</td>
<td>Development</td>
</tr>
<tr>
<td>4 IEEE1394.a</td>
<td>IEEE1394.a AV-protocol only (LINK + PHY)</td>
<td>Now</td>
<td>2005/6/E</td>
<td>2005/11/E</td>
<td>Development</td>
</tr>
<tr>
<td>5 S-ATA</td>
<td>S-ATA 1.5G Host PHY</td>
<td>2005.6.30(PHY)</td>
<td>2005.10.31(PHY)</td>
<td>2006.3.31(PHY)</td>
<td>Procurement</td>
</tr>
<tr>
<td>6 S-ATA</td>
<td>S-ATA 3.0G Host PHY</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>7 PCI-Express</td>
<td>PCI-Express 2.5G Endpoint PHY</td>
<td>2005.5.31(PHY)</td>
<td>2005.10.31(PHY)</td>
<td>2006.3.31(PHY)</td>
<td>Development</td>
</tr>
<tr>
<td>8 DRAM Controller</td>
<td>DDR2 400~533Mbps x 32</td>
<td>2005/5/E</td>
<td>2005/6/B</td>
<td>2005/9/E</td>
<td>Development</td>
</tr>
<tr>
<td>9 DRAM Controller</td>
<td>DDR2 400~533Mbps x 16</td>
<td>2005/5/E</td>
<td>2005/8/B</td>
<td>2005/11/E</td>
<td>Development</td>
</tr>
<tr>
<td>10 DDR2 ~800Mbps x 16</td>
<td>2005/9/B</td>
<td>2006/4/B</td>
<td>2006/8/E</td>
<td></td>
<td>Development</td>
</tr>
</tbody>
</table>

#### ARM

<table>
<thead>
<tr>
<th>Macro</th>
<th>Functions</th>
<th>Specifications</th>
<th>Design completion</th>
<th>Evaluation completion (SiliconProven)</th>
<th>Note (Procurement or Development)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ARM</td>
<td>ARM7TDMI–S</td>
<td>Now</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 ARM</td>
<td>ARM926EJ–S</td>
<td>Now</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 ARM</td>
<td>ARM946E–S</td>
<td>Now</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 ARM</td>
<td>ARM1176JZF–S</td>
<td>Now</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

We will deliver the library two months after the business fixation.
## PLL, DLL

### Table of Functions

<table>
<thead>
<tr>
<th>Macro</th>
<th>Functions</th>
<th>Specifications</th>
<th>Design completion</th>
<th>Evaluation completion (SiliconProven)</th>
<th>Note (Procurement or Development)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Fout:100–150MHz, Fin:12.5–150MHz, N=1–8, Power:1mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>2</td>
<td>Fout:150–200MHz, Fin:10–200MHz, N=1–15, Power:1mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>3</td>
<td>Fout:200–230MHz, Fin:10–200MHz, N=1–16, Power:1mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>4</td>
<td>Fout:100–300MHz, Fin:8–150MHz, N=2–38, Power:3mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>5</td>
<td>Fout:250–600MHz, Fin:8–200MHz, N=2–66, Power:4mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>6</td>
<td>Fout:400–800MHz, Fin:10–50MHz, N=12–40, Power:6mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>7</td>
<td>Fout:500–900MHz, Fin:6.25–150MHz, N=6–96, Power:6mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>8</td>
<td>Fout:600–1200MHz, Fin:6–80MHz, N=6–80, Power:7mW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Development</td>
</tr>
<tr>
<td>12</td>
<td>Fout:1200–1500MHz, Fin:24–100MHz, Power:10mW</td>
<td>2005/12/E</td>
<td>2005/12/E</td>
<td>2006/3/E</td>
<td>Development</td>
</tr>
<tr>
<td>14</td>
<td>Fout:24.576MHz, Fin:24KHz, N=1024, Power:10mW (High Multiply)</td>
<td>2005/6/E</td>
<td>2005/7/E</td>
<td>2005/12/E</td>
<td>Development</td>
</tr>
<tr>
<td>15</td>
<td>Fout:150–300MHz, Fin:18.75–37.5MHz, N=8, Power:15mW (SSC) (The available Fout[MHz]/Fin[MHz] pair is only five cases or 150/18.75,192/24,200/25,286/33,300/37.5)</td>
<td>2005/8/E</td>
<td>2005/8/E</td>
<td>2005/9/E</td>
<td>Development</td>
</tr>
</tbody>
</table>

*Analog Capacitor is 3.3V Poly-Diffusion capacitor.

### Table of Specifications

<table>
<thead>
<tr>
<th>Macro</th>
<th>Functions</th>
<th>Specifications</th>
<th>Design completion</th>
<th>Evaluation completion (SiliconProven)</th>
<th>Note (Procurement or Development)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Number of TAP:16, DQS≦133MHz, Power:10mW</td>
<td>NOW</td>
<td>Now</td>
<td>Now</td>
<td>Development</td>
</tr>
</tbody>
</table>

*Analog Capacitor is 3.3V Poly-Diffusion capacitor.
<table>
<thead>
<tr>
<th>Macro</th>
<th>Functions</th>
<th>Specifications</th>
<th>Design completion</th>
<th>Evaluation completion (SiliconProven)</th>
<th>Note (Procurement or Development)</th>
<th>Note VDD=3.3V(typ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>10bit 1MS/s</td>
<td>now</td>
<td>now</td>
<td>now</td>
<td>Development</td>
<td>Planning of Improvement Now Designing (with Input sw)</td>
</tr>
<tr>
<td>ADC</td>
<td>10bit 1MS/s</td>
<td>now</td>
<td>now</td>
<td>2005.9.E</td>
<td>Development</td>
<td>With 17ch Input Switch</td>
</tr>
<tr>
<td>ADC</td>
<td>6bit 108MS/s</td>
<td>now</td>
<td>now</td>
<td>2005.7.E</td>
<td>Development</td>
<td>Single Input</td>
</tr>
<tr>
<td>ADC</td>
<td>8bit 54MS/s</td>
<td>now</td>
<td>now</td>
<td>2005.7.E</td>
<td>Development</td>
<td>Single Input</td>
</tr>
<tr>
<td>ADC</td>
<td>10bit 30MS/s</td>
<td>now</td>
<td>now</td>
<td>2005.11.E</td>
<td>Development</td>
<td>Single Input</td>
</tr>
<tr>
<td>ADC</td>
<td>10bit 80MS/s</td>
<td>now</td>
<td>now</td>
<td>2005.10.E</td>
<td>Development</td>
<td>FMSL Differential Input</td>
</tr>
<tr>
<td>DAC</td>
<td>8bit 300kHz</td>
<td>now</td>
<td>now</td>
<td>now</td>
<td>Development</td>
<td>Voltage Output Low Power</td>
</tr>
<tr>
<td>DAC</td>
<td>8bit 1MHz</td>
<td>now</td>
<td>now</td>
<td>2005.7.E</td>
<td>Development</td>
<td>Voltage Output</td>
</tr>
<tr>
<td>DAC</td>
<td>10bit 300kHz</td>
<td>now</td>
<td>now</td>
<td>2005.7.E</td>
<td>Development</td>
<td>Voltage Output Low Power</td>
</tr>
<tr>
<td>DAC</td>
<td>10bit 1MHz</td>
<td>now</td>
<td>now</td>
<td>2005.7.E</td>
<td>Development</td>
<td>Voltage Output</td>
</tr>
<tr>
<td>DAC</td>
<td>10bit 30MHz</td>
<td>now</td>
<td>now</td>
<td>now</td>
<td>Development</td>
<td>Current Output VDD=2.5V</td>
</tr>
<tr>
<td>DAC</td>
<td>10bit 30MHz</td>
<td>now</td>
<td>now</td>
<td>2005.7.E</td>
<td>Development</td>
<td>Current Output With built-in resistance</td>
</tr>
<tr>
<td>DAC</td>
<td>10bit 54MHz</td>
<td>now</td>
<td>now</td>
<td>2005.11.E</td>
<td>Development</td>
<td>Current Output</td>
</tr>
</tbody>
</table>
THE POSSIBILITIES ARE INFINITE